IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 6-10 in accordance with the following:

1. (Previously Presented) A state indicating information setting circuit, comprising:

a first state holding part for inputting thereto a signal indicating either a predetermined first state or a predetermined second state, holding the state indicated by said signal input and outputting said state;

a second state holding part for inputting thereto the signal output from said first state holding part, holding the state indicated by said signal input and outputting said state;

a first state comparing part inputting thereto a predetermined state detection signal and the signal output from said second state holding part, and outputting a signal indicating said predetermined first state to said first state holding part when the respective states indicated by the respective signals input are different from one another, and outputting a signal indicating said predetermined second state when these states are same as one another;

a second state comparing part comparing the states of the respective signals output from said first state holding part and said second state holding part, and outputting a signal indicating said predetermined second state as a state detection signal clearing signal when the respective states indicated by said input signals are different from one another; and

a third state comparing part comparing the states of the respective signals output from said first state holding part and said second state holding part, outputting a state detection signal indicating said predetermined first state when said states of the respective signals input are different from each other, and outputting the state non-detection signal indicating said predetermined second state when said states are same as one another.

2. (Previously Presented) A state indicating information setting circuit, comprising:

a first state holding part inputting thereto a signal indicating either a predetermined first state or a predetermined second state, holding the state indicated by said signal input, and outputting said state;

a second state holding part inputting thereto the signal output from said first state holding part, and holding and outputting the state indicated by said signal input, and outputting said state;

a third state holding part inputting thereto the signal output from said second state holding part, and holding and outputting the state indicated by said signal input, and outputting said state;

a first state comparing part inputting thereto a predetermined state detection signal and the signal output from said second state holding part, outputting a signal indicating said predetermined first state to said first state holding part when the respective states indicated by the respective signals input are different from one another, and outputting a signal indicating said predetermined second state when these states are same as one another;

a second state comparing part comparing the states of the respective signals output from said first state holding part and said second state holding part, and outputting a signal indicating said predetermined second state as a state detection signal clearing signal when the respective states indicated by said input signals are different from one another; and

a third state comparing part comparing the states of the respective signals output from said first state holding part and said third state holding part, outputting a state detection signal indicating said predetermined first state when said states of the respective signals input are different from each other, and outputting the state non-detection signal indicating said predetermined second state when said states given are same as one another.

3. (Previously Presented) A state indicating information setting circuit, comprising:

a first state holding part holding a state of an input signal, and outputting a signal indicating said state thus held;

a second state holding part holding the state of the signal output from said first state holding part, and outputting a signal indicating said state thus held;

a state inverting part responsive to a predetermined state detection signal for outputting to said first state holding part a signal indicating a state which is different from the state indicated by the signal output from said second state holding part;

a state detection signal outputting part comparing the states of the respective signals output from said first state holding part and said second state holding part, outputting the state detection signal when said states are different from one another, and outputting a state non-detection signal when said states are same as one another; and

a state detection signal clearing part comparing the states of the respective signals

output from said first state holding part and said second state holding part, and outputting a state detection signal clearing signal when said states are different from one another.

4. (Previously Presented) A state indicating information setting circuit, comprising:

a first state holding part holding a state of an input signal, and outputting a signal indicating said state thus held;

a second state holding part holding the state of the signal output from said first state holding part, and outputting a signal indicating said state thus held;

a third state holding part holding the state of the signal output from said second state holding part, and outputting a signal indicating said state thus held;

a state inverting part responsive to a predetermined state detection signal for outputting to said first state holding part a signal indicating a state which is different from the state indicated by the signal output from said second state holding part;

a state detection signal outputting part comparing the states of the respective signals output from said first state holding part and said third state holding part, outputting the state detection signal when said states are different from one another, and outputting a state non-detection signal when said states are same as one another; and

a state detection signal clearing part comparing the states of the respective signals output from said first state holding part and said second state holding part, and outputting a state detection signal clearing signal when said states are different from one another.

5. (Previously Presented) A state indicating information setting circuit, comprising:

a first flip-flop circuit taking an input signal when a register read out signal has an L level;

a second flip-flop circuit taking a signal output from said first flip-flop circuit when the register read out signal has an H level;

a third flip-flop circuit taking a signal output from said second flip-flop circuit when the register read out signal has the L level;

a first exclusive-OR circuit performing an exclusive-OR operation between an output of said second flip-flop circuit and a predetermined state detection signal, and outputting a result of the exclusive-OR operation;

a second exclusive-OR circuit performing an exclusive-OR operation between an output of said first flip-flop circuit and an output of said second flip-flop circuit, and outputting a result of the exclusive-OR operation; and

a third exclusive-OR circuit performing an exclusive-OR operation between an output of

said first flip-flop circuit and an output of said third flip-flop circuit, and outputting a result of the exclusive-OR operation as a state bit signal.

6. (Currently Amended) A status bit setting circuit, comprising:

~~an inverting output part generating an output which is inverted each time that a predetermined status is detected;~~

~~state inversion transition parts, comprising edge-triggering type devices, having states inverted in sequence by the output of said inverting output part; and~~

~~a status bit setting part setting a predetermined status bit by detecting a process of propagation of the inversion transition in said state inversion transition parts~~

a first logic circuit which receives a status detection signal from an external status detecting part;

a first edge-triggering flip-flop circuit device which receives an output of the first logic circuit;

a second edge-triggering flip-flop circuit device which receives an output of the first edge-triggering flip-flop circuit device;

a third edge-triggering flip-flop circuit device which receives an output of the second edge-triggering flip-flop circuit device;

a second logic circuit which receives outputs of the first edge-triggering flip-flop circuit device and the second edge-triggering flip-flop circuit device;

a third logic circuit which receives outputs of the first edge-triggering flip-flop circuit device and the third edge-triggering flip-flop circuit device; and

a bus driver which receives an output of the third logic circuit and outputs a status bit signal.

7. (Currently Amended) The status bit setting circuit as claimed in claim 6, further comprising:

a status detection canceling part detecting ~~the~~a process of ~~the~~an inversion transition in said ~~state inversion transition parts~~first, second, and third edge-triggering flip-flop circuit devices and generating a signal canceling a status detection state.

8. (Currently Amended) The status bit setting circuit as claimed in claim 6, ~~wherein~~further comprising:

~~said~~a status bit setting part ~~detects~~detecting a completion of ~~the~~a propagation of ~~the~~an inversion transition in said first, second, and third edge-triggering flip-flop circuit devices and

~~cancels~~canceling the setting of ~~the~~a predetermined status bit.

9. (Currently Amended) The status bit setting circuit as claimed in claim 8, wherein:

said ~~state inversion transition parts~~first, second, and third edge-triggering flip-flop circuit devices have ~~the~~ states alternately inverted in sequence in response to a rising edge and a decaying edge of a predetermined read out signal.

10. (Currently Amended) The status bit setting circuit claimed in claim 6, ~~further comprising~~wherein:

~~a~~the bus driver ~~enabling~~enables reading out of ~~the~~a predetermined status bit externally only during an interval in which a predetermined read out signal is active.